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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,068	12/04/2003	Philipp Steinmann	TI-36776	7957

23494 7590 05/17/2005

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EXAMINER	
BOOTH, RICHARD A	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/728,068	STEINMANN ET AL.
	Examiner	Art Unit
	Nghia M. Doan	2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 12/04/2003.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-21 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-3,5-7 and 10-12 is/are rejected.

7)☒ Claim(s) 4,8,9,13-21 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 04 October 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12/04/2003.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Responsive to communication application filed on 12/04/2003, claims 1-21 are pending.

Claim Objections

1. Claim 15 is objected to because of the following informalities: as line 2, before "voltage", suggested that "vody" could be "body". Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1-3, 6,7, and 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lane et al. paper entitled "The design of Thin-Film polysilicon resistor for analog IC applications", in view of Applicant's Admitted Prior Art.**

4. **With respect to claim 1**, Lane et al. disclose a method of modeling a thin film resistor in an integrated circuit (abstract), comprising: characterizing a thermal resistance of the thin film resistor, wherein the thermal resistance accounts for self-heating thereof during operation (Lane et al. page 740, col. 2, ¶ 4, ll. 1-4); and

using the thermal resistance in a model for use in simulating integrated circuits using the thin film resistor (Lane et al. page 738, col. 2, ¶ 2, ll. 1-5 and ¶ 4, ll. 1-3).

5. Lane et al. do not teach fabricating the thin film resistor over a substrate and a dielectric.

Applicant's admitted prior art (AAPA) teaches the old and customized in the art of fabricating the thin film resistor over a substrate and a dielectric (Specification, page 1, ll. 15-22).

6. It would have been obvious to of ordinary skill in the art to combine the teaching of Lane with AAPA for suggestion an approach to designing polysilicon resistors of taking into account such electrical characteristics as a sheet resistance, temperature coefficient, voltage nonlinearity, uniformity, and matching (Lane et al. page 738, col. 2, ¶ 2, ll. 1-5). Therefore, the demonstrated that performance comparable to thin film resistor can be achieved without the requirement of a long time development time and specialized knowledge (Lane el at. page 738, col. 2, ¶ 3, ll. 11-14).

7. **With respect to claim 2**, Lane disclose the method of claim 1 , wherein characterizing the thermal resistance of the thin film resistor (Lane el at. page 740, col. 1, ¶ 1, ll. 1-3) comprises:

measuring dimensions of the thin film resistor (Lane el at. page 740, col. 1, ¶ 2, ll. 1-8); and

calculating an approximation of the thermal resistance using the measured dimensions (Lane el at. page 740, col. 2, ¶ 4, ll. 1-6; formulas 1,2; and page 741, col. 1, ll. 11-15; formulas 3, 4).

8. **With respect to claim 3**, Lane et al. teach the method of claim 2, wherein calculating the approximation of the thermal resistance comprises calculating the

thermal resistance as formulas (1) (Lane el at. page 740); (3), (5) (Lane el at. page 741).

9. Lane et al. do not explicitly teach the formula of claim 3. However, Lane et al. do disclose the formula as follow:

Substitute equations (3) and (5) into (1) and simplify, then $R_{th} = t_{ox}/(G_{ox}LW)$

While $t_{ox} = z$, and

$G_{ox} = \lambda$ (Lane el at. page 741, col. 1, ll. 4-6)

Therefore, according to the formula $R_{th} = t_{ox}/(G_{ox}LW)$ the teaching from Lane et al. is relevant and contains all elements of claimed formula below,

$R_{th} = z/\lambda LW$,

wherein R_{th} is the thermal resistance, z (t_{ox}) is a thickness of an electrically insulating layer overlying the substrate on which the thin film resistor resides, λ (G_{ox}) is the thermal conductivity distribution associated with the thin fill resistor, and L and W is the length and width of the thin film resistor, respectively.

10. Therefore, it would have been obvious to of ordinary skill in the art that even though Lane et al. do not use the Applicant's {exact/ precise} variables or expression for calculating thermal resistance, the formulas of Lane et al. can be rearranged to show how to calculate the thermal resistance, based on the structure characteristics of the thin film resistor (Lane et al. page 740, col. 1, ¶ 2, ll. 1-3).

11. **With respect to claim 6**, Lane et al. disclose the method of claim 1, further comprising fabricating a plurality of thin film resistors of the same type, wherein the

plurality of thin film resistors have varying dimensions associated therewith (Lane et al. page 738, col. 2, ¶ 4, ll. 6-11 and page 743, col. 1, ¶ 3, ll. 1-2).

12. **With respect to claims 7 and 10**, Lane et al. disclose the method of claim 6, wherein characterizing the thermal resistance of the thin film resistor comprises:

measuring a voltage/ current coefficient of the plurality of thin film resistors, thereby resulting in voltage/current coefficient data that reflects a change in resistance of the thin film resistors based on variations in applied voltage thereto (Lane et al. page 738, col. 1, Introduction, ll. 7-11; col. 2, ¶ 4, ll. 4-11); and

using the voltage/current coefficient data to extract fit parameters to characterize the thermal resistance (Lane et al. page 738, col. 2, ¶ 2, ll. 1-5).

However, the formulas (1), (3) and (5) mention as claim 6 suggest that calculating the thermal resistance of thin film resistance also relative to voltage and current coefficient (Lane et al. page 739, col. 1, ¶ 1, ll. 1-3).

Therefore, It would have been obvious to of ordinary skill in the art for the relationship between thermal resistance of the thin film resistor and voltage/ current coefficient that was well known in the Ohm's theory.

13. **With respect to claim 11**, Lane et al. disclose a method of modeling a bar-shaped thin film resistor, comprising:

forming a plurality of thin film resistors of differing sizes (Lane et al. page 738, col. 2, ¶ 4, ll. 6-11 and page 743, col. 1, ¶ 3, ll. 1-2);

measuring a voltage or current coefficient of the plurality of thin film resistors (Lane et al. page 738, col. 1, Introduction, ll. 7-11; col. 2, ¶ 4, ll. 4-11); and

determining a thermal resistance based on the measured voltage or current coefficient (Lane et al. page 738, col. 2, ¶ 2, ll. 1-5; fig. 4; page 741, col.1, ¶ 1; and col. 2, ¶ 2, ll. 4-6).

However, the formulas (1), (3) and (5) mention as claim 6 suggest that calculating the thermal resistance of thin film resistance also relative to voltage and current coefficient (Lane et al. page 739, col. 1, ¶ 1, ll. 1-3).

Therefore, It would have been obvious to of ordinary skill in the art for the relationship between thermal resistance of the thin film resistor and voltage/ current coefficient that was well known in the Ohm's theory.

14. **With respect to claim 12**, Lane et al. disclose the method of claim 11 , wherein measuring the voltage coefficients comprises:

applying a voltage of varying magnitude across the plurality of thin film resistors(page 738, col.2, ¶ 4, ll. 1-8) ; and

measuring a change in resistance of the plurality of thin film resistors as a function of the varied applied voltages (page 738, col.2, ¶ 4, ll. 8-11).

15. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lane et al. paper entitled "The design of Thin-Film polysilicon resistor for analog IC applications", in view of Joy et al. paper entitled " Thermal Properties of very Fast Transistor".

16. Lane et al. teach the method of claim 2, wherein calculating the approximation of the thermal resistance comprises calculating the thermal resistance according to the formula disclose in claim 5,

$R_{th} = z/\lambda LW$

wherein R_{th} is the thermal resistance, z is a thickness of an electrically insulating layer overlying the substrate on which the thin film resistor resides, λ is the thermal conductivity distribution associated with the thin film resistor, and L and W are the length, and width of the thin film resistor, respectively.

17. Lane et al. also teach formulas (1) through (7) , that associated for calculate the thermal resistance of the thin film resistor

18. Lane et al. do not teach R_{th} relative to the height of thin film resistor,

19. Joy et al. teach thermal resistance of thin film, which is bar shape (fig. 10) associated with L, W, and H are the length, width, and height of the thin film (Joy, page 587, col. 2, ll. 5-12) , respectively.

20. However, combining the teaching of Lane et al. (formulas (1) through (7)) with Richard et al. (formulas (11) and (12) may be derived that at least suggests, if not disclose the thermal resistance of the thin film resistor according to the claimed formula as below:

$R_{th} = z/\lambda\,(LW + 2H(L + W))$,

21. Therefore, it would have been obvious to of ordinary skill in the art to reference Joy in determining the effect of the thermal spreading resistance because Joy disclose

additional that involve change in the size and depth of the dissipating region (Richard, page 592, col. 1, ¶ 4, ll. 2-4) .

Allowable Subject Matter

22. **Claims 4, 8, 9, and 13- 21** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

23. The following is a statement of reasons for the indication of allowable subject matter: **regarding to claims 4, 8, 9**, the prior arts do not teach " a fit parameter that account for a temperature gradient associated with top, peripheral, bottom portions for calculating a thermal resistance of the thin film resistor" .

24. The following is a statement of reasons for the indication of allowable subject matter: **regarding to claims 13-21**, the prior arts do not teach "using body voltage coefficient, head voltage coefficient data to calculate a voltage coefficient and thermal resistance for thin film resistor"

Conclusion

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Chung et al. and Pence et al. reference for teaching a method of measuring a thermal resistance associated with geometrical of thin film resistor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NMD

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